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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/800,180

03/12/2004

Yi Chung

8071-55 (OPP 030490US)

8614

7590

06/30/2004

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EXAMINER

YEVSNIKOV, VICTOR V

ART UNIT

PAPER NUMBER

2825

DATE MAILED: 06/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/800,180

Applicant(s)

CHUNG, YI

Examiner

Victor V Yevsikov

Art Unit

2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 12 March 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-7 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-7 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☒ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1, 2 and 4 are rejected under 35 U.S.C. 102(a) as being anticipated by Kim et al. (U.S. 2003/0223019 A1).

With respect to claims 1, 2 and 4 Kim teaches a thin film transistor array panel comprising:

- a substrate 110;
- a gate electrode 124;
- a gate insulating layer 140 formed on the gate electrode 124;
- a polysilicon layer 154 formed on the gate insulating layer 140 and including a pair of ohmic contact areas 163, 165 doped with n type conductive impurity;
- source 173 and drain 175 electrodes formed on the ohmic contact areas 163, 165 at least in part;
- a passivation layer 180 formed on the source and the drain electrodes and having a contact holes 181-183 exposing the drain electrode at least in part; and
- a pixel electrode 190 formed on the passivation layer and connected to the drain

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electrode 175 through the contact hole 183, wherein:

the conductive impurity comprises boron or phosphorous;

a gate line disposed between the substrate and the gate insulating layer and connected to the gate electrode; and a data line disposed between the gate insulating layer and the passivation layer and connected to the source electrode.

Reference: abstract; fig. 2 with corresponding text.

Claims 5 – 7 are rejected under 35 U.S.C. 102(a) as being anticipated by Park (U.S. 2002/0097349 A1).

With respect to claims 5-7 Park teaches a method of manufacturing a thin film transistor array panel, the method comprising:

forming a gate electrode 24;

depositing a gate insulating layer 30 and a polysilicon layer 40 on the gate electrode in sequence;

forming a photoresist having a first portion 112 and a second portion 114 thinner than the first portion on the polysilicon layer;

patterning the polysilicon layer using the photoresist as a mask to form a semiconductor layer 40;

removing the second portion of the photoresist;

performing impurity implantation using the first portion of the photoresist as a mask to form ohmic contact areas in the semiconductor layer;

removing the first portion of the photoresist;

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forming source 65 and drain 66 electrodes on the ohmic contact areas;  
forming a passivation layer 72 having a contact hole 71 on the drain electrode;  
and  
forming a pixel electrode 82 on the passivation layer; and wherein:  
the formation of the photoresist comprising coating a photoresist film on the polysilicon layer;  
exposing the photoresist film through a photo-mask having a slit pattern or a translucent portion facing the second portion of the photoresist;  
developing the photoresist film to form the photoresist;  
the impurity comprises p type conductive impurity.  
Reference: figs. 3, 5A-5g with corresponding text.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 3 is rejected as being prima facie obvious without showing that the claimed impurity ranges achieve unexpected results relative to the prior art range.

In re Woodruff, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also In re Huang, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996) (claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new

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and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also *In re Boesch*, 205 USPQ 215 (CCPA 1980) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and *In re Aller*, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious).

Therefore, to select the top silicon layer as being thicker is seen as an obvious development over prior art as the changing of dimension has not been shown to produce unexpected results.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor Yevsikov whose telephone number is (571) 272-1910. The examiner can normally be reached on Monday –Thursdays 8:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, examiner's supervisor, Matthew S. Smith, can be reached on (571) 272-1907. The fax phone numbers for the organization where this application or processing is assigned is (703) 873-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published application may be obtained from either Private PAIR or Public PAIR. Status information for unpublished application is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on

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access to the Private PAIR system, contact the Electronic Business Center (EBC) at  
866-217-9197 (toll-free).

*V. Yevsikov*

Victor Yevsikov

Examiner

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June 22, 2004

*C. Everhart*  
CARIDAD EVERHART  
PRIMARY EXAMINER